Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.



**.024”**

**.024”**

**Top Material: Al**

**Backside Material: Au**

**Bond Pad Size: .004” X .004”**

**Backside Potential: Collector**

**Mask Ref: DAC**

**APPROVED BY: DK DIE SIZE .024” X .024” DATE: 7/7/22**

**MFG: ALLEGRO-SPRAGUE THICKNESS .012” P/N: MPSA06**

**DG 10.1.2**

#### Rev B, 7/1